Docket No.: 4425-343 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
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Chih-Yung CHEN *et al.*	:	Confirmation No. 2606
	:	
U.S. Patent Application No. 10/765,897	:	Group Art Unit: 2188
	:	
Filed: January 29, 2004	:	Examiner: David Masdon

For: A SYSTEM CHIP RELATED METHOD OF DATA ACCESS

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Appellant submits the enclosed replacement section SUMMARY OF CLAIMED SUBJECT MATTER in response to the Notification of Non-Compliant Appeal Brief dated December 13, 2007.

V) SUMMARY OF CLAIMED SUBJECT MATTER

For the purpose of this appeal brief only, the claimed subject matter will be explained herein below with references to the specification by page and line number, and to the drawings by reference characters.

Independent **Claim 1** is directed to a data access apparatus (20, 21, 22, FIGs. 2A and 2B), comprising:

an external memory unit (21, FIGs. 2A and 2B) for storing data, wherein the external memory unit (21) has a second time cycle (302, FIG. 3) for performing a task;[1] and

a control unit (20, FIGs. 2A and 2B) coupled with the external memory unit (21) via a memory bus (22, FIGs. 2A and 2B),[2]

said control unit (20) comprising:

a microprocessor unit (201A, FIGs. 2A and 2B), having a first time cycle (304, FIG. 3) to perform a microprocessor operating;[3] and

a memory interface control unit (203, FIGs. 2A and 2B) for correspondingly transforming an internal data access address of an internal memory unit (202, FIGs. 2A and 2B), which is accessible only by the microprocessor unit (201A), into a data address of the external memory unit (21), thereby the microprocessor unit (201A) issuing the internal data access address could access data from the external memory unit (21) via the memory interface control unit (203);[4]

wherein

the external memory unit (21) has a data segment (210, FIG. 2B) storing flow control parameters and numerical arithmetic of the microprocessor unit (201A),[5] and

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[1] See, for example, page 4, lines 25-26, and page 6, lines 18-19.
[2] See, for example, page 5, lines 9-10.
[3] See, for example, page 7, lines 23-24.
[4] See, for example, page 5, lines 10-16, page 6, lines 23-26, and page 7, lines 1-2.
[5] See, for example, page 5, lines 21-23.

when the microprocessor unit (201A) attempts to access the data segment (210) storing flow control parameters and numerical arithmetic from the external memory unit (21), an access request signal (308, FIG. 3) issued from the control unit (20) associated with the microprocessor unit (201A) against another device (204, FIGs. 2A and 2B)[6] accessing the external memory unit (21) is directed to the external memory unit (21), and the first time cycle (304) is suspended until an acknowledge signal (312, FIG. 3) indicating that the microprocessor unit (201A) may access the data segment (210) of the external memory unit (21) is received.[7]

Independent **Claim 8** is directed to a control unit (20, FIGs. 2A and 2B) for accessing data from an external memory unit (21, FIGs. 2A and 2B), having a second time cycle (302, FIG. 3), via a memory bus (22, FIGs. 2A and 2B) in an optical-electronic system,[8]

the control unit (20) comprising:

a microprocessor unit (201A, FIGs. 2A and 2B) having a first time cycle (304, FIG. 3) to perform a microprocessor operation;[9] and

a memory interface control unit (203, FIGs. 2A and 2B) for correspondingly transforming an internal data access address of an internal memory unit (202, FIGs. 2A and 2B), which is accessible only by the microprocessor unit (201A), into a data address of the external memory unit (21), thereby the microprocessor unit (201A) issuing the internal data access address could access data from the external memory unit (21) via the memory interface control unit (203);[10]

wherein

when the microprocessor unit (201A) attempts to access data from the external memory unit (21) via the memory interface, the control unit (20) is operable to send an access request signal (308, FIG. 3) to the external memory unit (21),[11]

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[6] See, for example, page 8, lines 4-6.
[7] See, for example, page 7, lines 11-24.
[8] See, for example, page 5, lines 9-10, and page 6, lines 18-19.
[9] See, for example, page 7, lines 23-24.
[10] See, for example, page 5, lines 10-16, page 6, lines 23-26, and page 7, lines 1-2.
[11] See, for example, page 7, lines 11-14.

flow control parameters and numerical arithmetic of the microprocessor unit (201A) is stored in a data segment (210, FIG. 2B) within the external memory unit (21),[12] and

when the microprocessor unit (201A) attempts to access the data segment (210) storing flow control parameters and numerical arithmetic from the external memory unit (21), the access request signal (308) issued from the control unit (20) associated with the microprocessor unit (201A) against another device (204, FIGs. 2A and 2B)[13] accessing the external memory unit (21) is directed to the external memory unit (21), and the first time cycle (304) is suspended until an acknowledge signal (312, FIG. 3) indicating that the microprocessor unit (201A) may access the data segment (210) of the external memory unit (21) is received.[14]

Independent **Claim 15** is directed to a data access method used in a control unit (20, FIGs. 2A and 2B) for accessing data in an external memory unit (21, DIGs. 2A and 2B),[15]

said method comprising:

correspondingly transforming an internal data access address of an internal memory unit (202, FIGs. 2A and 2B), which is accessible only by a microprocessor unit (201A, FIGs. 2A and 2B) of the control unit (20), into a data address of the external memory unit (21), thereby the microprocessor (201A) issuing the internal data access address could access data from the external memory unit (21);[16]

suspending (400, FIG. 4) a first time clock (304, FIG. 3) used by the microprocessor (201A) of the control unit (20) when the microprocessor (201A) sends an access request signal (308, FIG. 3) for accessing a data segment (210, FIG. 2B) in the external memory unit (21), wherein the data segment (210) stores flow control parameters and numerical arithmetic of the microprocessor unit (201A), and wherein the access request signal (308) issued from the control unit (20) associated with the

[12] See, for example, page 5, lines 21-23.
[13] See, for example, page 8, lines 4-6.
[14] See, for example, page 7, lines 11-24.
[15] See, for example, page 5, lines 12-14.
[16] See, for example, page 5, lines 10-16, and page 6, lines 23-26.

microprocessor unit (201A) against another device (204, FIGs. 2A and 2B)[17] accessing the external memory unit (21) is directed to the external memory unit (21);[18] and

reviving (406, FIG. 4) the first time clock (304) when an acknowledge signal (312, FIG. 3) indicating that the microprocessor unit (201A) may access the data segment (210) of the external memory unit (21) is received.[19]

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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[17] See, for example, page 8, lines 4-6.
[18] See, for example, page 5, lines 21-23, page 7, lines 11-20, and page 9, lines 5-6.
[19] See, for example, page 7, lines 20-22, and page 9, lines 9-11.